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Description. The design of today's semiconductor chips for various applications, such as telecommunications, poses various challenges due to the complexity of these systems. These highly complex systems-on-chips demand new approaches to connect and manage the communication between on-chip processing and storage components and networks on chips (NoCs) provide a powerful solution.

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Networks on chips are designed using principles that investigated for multiprocessor computers as well as for local and wide area networks. Networks are characterized by architectures and protocols. The former embody the structural relations among the constituents of the network, while the latter specify the ways in which the network operates under various conditions.

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To address these limitations, the network-on-chip (NoC) introduces a packet-switched fabric for on-chip communication, and it becomes the de facto many-core interconnection mechanism. The baseline NoC design exploration mainly consists of the design of the network topology, routing algorithm, flow control mechanism, and router microarchitecture.

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Gupta, U & Ogras, U 2016, Extending networks from chips to flexible and stretchable electronics. in 2016 10th IEEE/ACM International Symposium on Networks-on-Chip, NOCS 2016., 7579341, Institute of Electrical and Electronics Engineers Inc., 10th IEEE/ACM International Symposium on Networks-on-Chip, NOCS 2016, Nara, Japan, 8/31/16.

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A network on a chip or network-on-chip (NoC / ˌ ɛ n ˌ oʊ ˈ s iː / en-oh-SEE or / n ɒ k / knock) is a network-based communications subsystem on an integrated circuit ("microchip"), most typically between modules in a system on a chip (SoC). The modules on the IC are typically semiconductor IP cores schematizing various functions of the computer system, and are designed to be modular in ...