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The current activities in the design of testable/fault tolerant integrated circuits are reviewed and areas for future emphasis are suggested. The rapid evolution of high performance Very Large Scale Integrated Circuits (VLSICs) has resulted in accelerated opportunities for improving the operational performance of military electronic systems. ...

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Fault tolerance as a property finds application in a wide variety of scenarios ranging from satellites to modern microprocessors. Fault tolerant systems have the capability of withstanding defects and are able to provide specified output despite faults occurring or having occurred. Similarly design for testability (DFT) is a technique that ...

Defect/Fault Tolerant Systems and Design for Testability ...
Students are responsible for: homework and 1-page paper summaries - 35% of grade midterm exam - 20% of grade final exam - 25% of grade individual or group project (due at beginning of class on specified day) - 20% of grade

ECE 254 / CPS 225 - Fault-Tolerant and Testable Computing ...
Objective: To provide students with an understanding of fault tolerant computers, including both the theory of how to design and evaluate them and the practical knowledge of real fault tolerant systems.

ECE/CS 554 - Fault-Tolerant and Testable Computing Systems
Another variation of this problem is when fault tolerance in one component prevents fault detection in a different component. For example, if component B performs some operation based on the output from component A, then fault tolerance in B can hide a problem with A.

Fault tolerance - Wikipedia
Fault tolerant and fault testable hardware design March 1985. March 1985. Read More. Author: Parag K. Lala. Syracuse Univ., Syracuse, NY. Publisher: Prentice-Hall, Inc. Division of Simon and Schuster One Lake Street Upper Saddle River, NJ; United States; ISBN: 978-0-13-308248-7. Available at Amazon.

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Features A systematic study of the various fault tolerant architectures in use. An in depth review of the basic characteristics of self checking logic detailed descriptions of all the major hardware techniques that may be used in fault tolerant and testable design.

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Fault tolerant and fault testable hardware design This edition published in 1985 by Prentice-Hall International in Englewood Cliffs, N.J.

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Fault-tolerant and self-testable architectures for zero failure electronics Richardson, A and Sharif, E and Betts, W R (1997) Fault-tolerant and self-testable architectures for zero failure electronics. In: AUTOMOTIVE ELECTRONICS - AUTOTECH'97. IMechE seminar publication ; 1997-10.

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