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Q. 4.1: Consider the combinational circuit shown in Fig. P4.1.(a) Derive the Boolean*

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~~expressions fo Q. 4.7: Design a combinational circuit that converts a four bit Gray code (Table 1.6) to a bit four Q. 4.26: Construct a 4 to 16 line decoder with five 2 to 4 line decoders with enable. Q. 4.23: Draw the logic diagram of 2-to-4-line decoder~~

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using (a) NOR gates only (b)

NAND gates only **Design of 4×4 RAM || Construction of a 4×4 RAM || RAM in computer architecture | 4×4 RAM design**
Q. 4.3: For the circuit shown in Fig. 4.33 (Section 4.11), (a) Write the Boolean functions

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Q. 1.1: List the octal and hexadecimal numbers from 16 to 32. Using A and B for the last two digits *Q. 4.8: Design a code converter that converts a decimal digit from the 8, 4, -2, -1 code to BCD* *Q. 3.29: Implement the following four Boolean*

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expressions with three half adders: $D=A\oplus B\oplus C$ Q. 4.4: Design a combinational circuit with three inputs and one output. (a) The output is 1 when Q. 6.7: Draw the logic diagram of a four-bit register with four D flip-flops and four 4×1 multiple Learn how to create an

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~~Implement boolean function using decoder~~ **state diagram/state table/circuit diagram (using D-flip flop) - Digital Logic Design**

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Combinational circuit with decoder and external logic gates - Digital Electronics Example

Lesson 11 - VHDL Example 3:
Majority Circuit

Lesson 14 - PLDs and CPLDs
Sequential Circuit Analysis - From sequential circuit to state

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in5 Q. 5.10: A sequential circuit has two JK flip-flops A and B, two inputs x and y, and one output z

Lecture 4: Digital Logic Gates

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قطن م ل ا م ي م ص ت ي ب ر ع ل ا ب ح ر ش -

Q. 5.6: A sequential circuit with two D flip-flops A and B, two inputs, x and y; and one output z is

Q. 5.1: The D latch of Fig. 5.6 is constructed with four NAND gates and an inverter.

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Consider the *Digital Logic Design - Unit 04 - Combinational Logic - Part 03 - Design Procedure*

Q. 3.6: Simplify the following Boolean expressions, using four-variable maps: (a) $A'B'C'D' + AC'D'$ + Q. 4.37: Implement the following Boolean function with a

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4 * 1 multiplexer and external gates **Q. 4.35: Implement a full adder with two 4 * 1 multiplexers.** Digital Design Morris Mano 4th

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