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The Cadence 3D Design Viewer is a full, solid model 3D viewer and 3D wirebond DRC solution for complex IC package designs. It allows users to visualize and investigate an entire design, or a selected design subset, such as a die stack or complex via array. It provides a common reference point for design reviews. OTHER SIP DIGITAL SOLUTION PRODUCTS

CADENCE SIP DIGITAL ARCHITECT - FlowCAD
Cadence PCB Solutions Cadence® 3D Design Viewer is a full, solid model 3D viewer and 3D wire bond design rule checking (DRC) solution for complex IC package designs that is tightly integrated and included with Cadence SiP Layout. It is also available separately to be used standalone or tightly integrated with Allegro® Package Designer (APD).

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The AWR Connected™for Cadence Allegro solution integrates Cadence Allegro multi-chip module (MCM), system in package (SiP), PCB, and package layout tools with AWR Design Environment Microwave Office circuit design software. The flow works by extracting user-

Datasheet AWR Connected for Cadence Allegro
Explore Cadence IP. For the past five ... (SiPs), that is adding several different chips into one package. The next hurdle for our industry was processor-to-memory latency reduction. To try to address that issue, we started seeing package-level implementation and silicon interposers in 2008. An interposer is essentially a silicon chip that acts as electrical interface, routing electrical ...